REMARKS

Claims 1-20 were examined and reported in the Office Action. Claims 1, 2, 19 and 20 are rejected. Claims 1-20 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 102(e)

It is asserted in the Office Action that claims 1, 2, 19-20 are rejected under 35 U.S.C. § 102(e), as being anticipated by U. S. Patent Application No. 2003/0107928 issued to Sakata ("Sakata"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131,

> '[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Sakata discloses replacement decisions are performed in order that a second replacement region can be made smaller than a first replacement and that the second replacement is given priority over the first replacement. The first replacement is controlled by a repair address of a small number of bits. Sakata, however, fails to teach, disclose or suggest a signal controller for generating control signals and an enable signal; and an address latch unit for latching an input address in response to the control signals.

It is asserted in the Office Action that a control circuit RMCU and an address buffer AB of Sakata corresponds to the signal controller 500 and the address latch unit 400 of Applicant's claimed invention, respectively. However, referring to Figs. 4, 5 and 7 of Sakata, no output of a

column-side repair decision circuit YR including the control circuit RMCU is input to the address buffer AM. That is, an operation of the address buffer AB is not controlled by outputs of the control circuit RMCU. Therefore, it is clear that the control circuit RMCU and the address buffer AB of Sakata are totally different from the signal controller 500 and the address latch unit 400 of the present invention.

Further, Sakata fails to teach, disclose or suggest a comparator delay modeling block for delaying an enable signal output from the signal controller for a predetermined time. It is asserted in the Office Action that a one-bit comparator AC1 corresponds to the comparator delay modeling block 700 of Applicant's claimed invention. Sakata discloses that the one-bit comparator AC1 compares the repair address, i.e., the output of the fuse decision circuit, with the input row address (see Sakata paragraph [0064]). That is, an operation of the one-bit comparator AC1 is completely distinguishable from delaying the enable signal. Moreover, the comparator delay modeling block 700 of Applicant's claimed invention only delays an enable signal RAE_FUSE output from the signal controller 500 and does not perform a comparing operation.

Therefore, Applicant asserts that the one bit comparator AC1 of Sakata cannot be considered to perform the same operation as the comparator delay modeling block of Applicant's claimed invention.

Since Sakata does not teach, disclose or suggest all of Applicant's claims 1 and 19 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Sakata. Thus, Applicant's claims 1 and 19 are not anticipated by Sakata. Additionally, the claims that directly or indirectly depend on amended claims 1 and 19, namely claims 2, and 20, respectively, are also not anticipated by Sakata for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejections for claims 1, 2, and 19-20 are respectfully requested.

II. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 3-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-20, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-20 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: April 11, 2007

By: _____

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

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Jean Svoboda Date: April 11, 2007